

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A monolithic semiconductor device comprising:

a semiconductor substrate;

a plurality of microstructures formed over the substrate, wherein the microstructures are stud capacitors;

a brace transversely extending between lateral sides of at least two of the microstructures; and

a vertical space between said brace and said semiconductor substrate.

2. (Original) The semiconductor device according to claim 1, wherein the brace interconnects substantially all of the microstructures.

3. (Original) The semiconductor device according to claim 1, where the brace is located substantially near upper ends of the microstructures.

4. (Withdrawn) The semiconductor device according to claim 1, wherein the brace has a width approximately equal to or less than the largest cross-sectional dimension of the microstructures.

5. (Original) The semiconductor device according to claim 1, wherein the brace comprises a microbridge structure extending above the substrate and between two or more of the microstructures.

6. (Original) The semiconductor device according to claim 1, where the microstructures each comprise a conductor material portion standing upright over the substrate, and wherein the brace interconnects the conductor material portions of two or more of the microstructures.

7. (Withdrawn) The semiconductor device according to claim 1, wherein the microstructures comprise generally cylindrical container shapes and the brace comprises a microbridge structure.

8. (Original) The semiconductor device according to claim 1, wherein the microstructures comprise generally solid cylindrical shapes and the brace comprises a microbridge structure.

9. (Original) The semiconductor device according to claim 1, where the brace comprises a dielectric material.

10. (Original) The semiconductor device according to claim 1, further comprising a dielectric layer between the substrate and the brace, where the brace is vertically spaced from the dielectric layer.

11. (Original) The semiconductor device according to claim 1, wherein the microstructures comprise conductive material and the brace comprises a dielectric.

12. (Withdrawn) The semiconductor device according to claim 1, wherein the microstructures are defined within an active circuit area, and further comprising a die having non-active circuit areas located adjacent the active circuit area, wherein the brace further interconnects at least two of the microstructures with non-active areas of the die.

13. (Cancelled).

14. (Withdrawn) The semiconductor device according to claim 1, wherein the microstructures are container capacitors.

15. (Withdrawn) The semiconductor device according to claim 1, wherein the microstructures comprise double-sided container capacitors.

16. - 22. (Cancelled).

23. (Previously Presented) A semiconductor storage capacitor, comprising:

a semiconductor substrate;

a plurality of capacitor storage node microstructures formed over the substrate; and

a brace transversely extending between lateral sides of at least two of the microstructures, wherein the microstructures comprise generally solid cylindrical shapes and the brace comprises a microbridge structure,

and wherein there is a vertical space between said brace and said semiconductor substrate.

24. - 27. (Cancelled).

28. (Previously Presented) A semiconductor storage capacitor, comprising:

a semiconductor substrate;

capacitor storage node microstructures formed over the substrate;

and

a brace transversely extending between lateral sides of at least two of the microstructures, wherein the microstructures comprise stud capacitors, and wherein there is a vertical space between said brace and said semiconductor substrate.

29. - 38. (Cancelled).

39. (Previously Presented) A memory circuit, comprising:

a semiconductor substrate having a memory cell including diffusion regions;

a dielectric layer on the substrate;

conductive plugs extending vertically from an upper surface of the dielectric layer to respective diffusion regions;

capacitor storage node microstructures each formed over the dielectric layer and a respective conductive plug; and

a brace transversely extending between and laterally supporting respective lateral sides of at least two of the microstructures, wherein the microstructures comprise generally solid cylindrical shapes and the brace comprises a microbridge structure, and wherein there is a vertical space between said brace and said semiconductor substrate.

40. - 43. (Cancelled).

44. (Previously Presented) A memory circuit, comprising:

a semiconductor substrate having a memory cell including diffusion regions;

a dielectric layer on the substrate;

conductive plugs extending vertically from an upper surface of the dielectric layer to respective diffusion regions;

capacitor storage node microstructures each formed over the dielectric layer and a respective conductive plug; and

a brace transversely extending between and laterally supporting respective lateral sides of at least two of the microstructures, wherein the microstructures comprise stud capacitors, and wherein there is a vertical space between said brace and said semiconductor substrate.

45. - 76. (Cancelled).

77. (Previously Presented) A processor system, comprising:

a processor; and

a memory circuit fabricated on a semiconductor chip
communicating with the processor, said memory circuit comprising:

a semiconductor substrate having a memory cell including
diffusion regions;

a dielectric layer on the substrate;

conductive plugs extending vertically from an upper surface of the
dielectric layer to respective diffusion regions;

capacitor storage node microstructures each formed over the
dielectric layer and a respective conductive plug; and

a brace transversely extending between and laterally supporting
respective lateral sides of at least two of the microstructures, wherein the
capacitor microstructures comprise capacitor studs, wherein there is a
vertical space between said brace and said semiconductor substrate.

78. (Currently Amended) A support structure on a semiconductor
device comprising:

a plurality of braces transversely extending between lateral sides of
a microstructure[[s]] formed over a semiconductor substrate, said

microstructure comprising a generally solid cylindrical shape, wherein said plurality of braces comprise a support structure for said [[plurality of]] microstructure[[s]]; and

a vertical space between said plurality of braces and said semiconductor substrate.

79. (Currently Amended) A brace for a semiconductor device comprising:

at least one brace transversely extending between lateral sides of at least two microstructures on a semiconductor substrate, said at least two microstructures comprising stud capacitors, wherein said at least two microstructures are supported only by said at least one brace, wherein said at least one brace comprises one material layer.

80. (Currently Amended) An in-process semiconductor device comprising:

a semiconductor substrate;

at least two microstructures formed over the substrate, said at least two microstructures comprising generally solid cylindrical shapes; and

at least one brace transversely extending between lateral sides of said at least two microstructures, wherein said at least two [[of said plurality of]] microstructures are supported only by said at least one

brace, and wherein said at least one brace comprises a single material layer.

81. (Currently Amended) A semiconductor support structure, comprising:

a semiconductor substrate;

microstructures formed over the substrate; and

[[at least one]] a plurality of braces transversely extending between lateral sides of at least two of the microstructures, wherein the plurality of braces comprise[[s]] a lattice support structure wherein said plurality of braces intersect at said microstructures, and wherein there is a vertical space between said support structure and said semiconductor substrate.

82. (Cancelled).

83. (Cancelled).

84. (Previously Presented) A semiconductor storage capacitor, comprising:

a semiconductor substrate;

a plurality of capacitor storage node microstructures formed over the substrate, said microstructures having vertical surfaces;

a brace transversely extending between the vertical surfaces of at least two of the microstructures, said brace being located substantially near the upper ends of said vertical surfaces of said microstructures; and

a vertical space between said brace and said substrate.

85. (Previously Presented) A semiconductor storage capacitor, comprising:

a semiconductor substrate;

capacitor storage node microstructures formed over the substrate, said microstructures having vertical surfaces; and

a plurality of braces transversely extending between the vertical surfaces of at least two of the microstructures, said plurality of braces being located substantially near the upper ends of said vertical surfaces of said microstructures, and wherein there is a vertical space between said plurality of braces and said semiconductor substrate.